

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Brent Keeth

Serial No.: Not yet assigned

Filed: July 14, 2003

For: DIGIT LINE ARCHITECTURE FOR
DYNAMIC MEMORY

Examiner: Unknown

Group Art Unit: Unknown

Attorney Docket No.: 3351.8US
(96-0223.07/US)

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INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

The present application is a continuation of application Serial No. 10/150,236, filed May 17, 2002, pending, which is a continuation of application Serial No. 09/826,764, filed April 5, 2001, now U.S. Patent 6,392,303 B2, issued May 21, 2002, which is a continuation of application Serial No. 09/507,170, filed February 18, 2000, now U.S. Patent 6,243,311, issued June 5, 2001, which is a divisional of application Serial No. 08/701,749, filed August 22, 1996, now U.S. Patent 6,043,562, issued March 28, 2000. This application claims priority to provisional application serial numbers 60/010,293 filed February 1, 1996, and 60/010,622 filed January 26, 1996.

Pursuant to M.P.E.P. 2001.06(b), the Examiner is respectfully requested to consider the information of record in the prior applications, and to confirm in the first Office Action on the merits that such art has in fact been reviewed. A PTO-1449 form listing all of the information of record in the prior applications is enclosed herewith.

This Information Disclosure Statement is filed within three (3) months of the filing date of the above-identified application, and no certification pursuant to 37 C.F.R. § 1.97(c) or a fee pursuant to 37 C.F.R. 1.17(p) is required.

Respectfully submitted,



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Date: July 14, 2003

JRD/sls:djp

Enclosure: Form PTO-1449

Form PTO-1449 INFORMATION DISCLOSURE CITATION IN AN APPLICATION <i>(Use several sheets if necessary)</i>			Docket Number (Optional) 3351.8US (96-0223.07/US)		Application Number Not yet assigned	
			Applicant Brent Ke th			
			Filing Date July 14, 2003		Group Art Unit Unknown	

U.S. PATENT DOCUMENTS						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4,536,947	08/1985	Bohr et al.			
	4,742,018	05/1988	Kimura et al.			
	4,914,502	04/1990	Lebowitz et al.			
	4,922,460	05/1990	Furutani et al.			
	4,967,396	10/1990	Kajigaya et al.			
	4,970,564	11/1990	Kimura et al.			
	5,014,110	05/1991	Satoh			
	5,107,459	04/1992	Chu et al.			
	5,138,412	08/1992	Hieda et al.			
	5,170,243	12/1992	Dhong et al.			
	5,206,183	04/1993	Dennison			
	5,208,180	05/1993	Gonzalez			
	5,243,558	09/1993	Saeki			

FOREIGN PATENT DOCUMENTS							
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO
	3-174765	07/1991	Japan				
	60-258795	12/1984	Japan				
	4433695	03/1995	Germany				
	0078338	05/1983	EPO				

OTHER DOCUMENTS		(Including Author, Title, Date, Pertinent Pages, Etc.)
		Ahn et al., "Bidirectional Matched Global Bit Line Scheme for High Density DRAMS", (Abstract), pps. 91-92.
		Hamada et al., "A Split -Level Diagonal Bit-Line (SLDB) Stacked Capacitor Cell for 256MbDRAMs", IEEE, April; 1992, pps. 799-802.
		Inoue et al., "A 16Mb DRAM with An Open Bit-Line Architecture", International Solid State Circuits Conference, IEEE, 1988, pps. 246-247.

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance not considered. Include copy of this form with next communication to the applicant.

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)
3351.8US (96-0223.07/US)

Application Number
Not yet assigned

Applicant **Brent Keeth**

Filing Date **July 14, 2003**

Group Art Unit **Unknown**

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5,280,443	01/1994	Hidaka et al.			
	5,315,542	05/1994	Melzner			
	5,396,450	03/1995	Takashima et al.			
	5,396,451	03/1995	Ema			
	5,499,205	03/1996	Ahn et al.			
	5,534,732	07/1996	DeBrosse et al.			
	5,581,126	12/1996	Moench			
	5,625,234	04/1997	Suzuki et al.			
	5,670,815	09/1997	Childs et al.			
	5,680,347	10/1997	Takeuchi et al.			
	5,815,428	09/1998	Tsuruda et al.			
	5,838,038	11/1998	Takashima et al.			
	5,864,181	01/1999	Keeth			
	5,877,976	03/1999	Lattimore et al.			

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	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

		Kimura et al., "A Block-Oriented RAM with Half-Sized DRAM Cell and Quasi-Folded Data-Line Architecture", November 11, 1991, IEEE, Journal of Solid-State Circuit, pps. 1511-1518.
		Takashima et al., "Open/Folded Bit-Line Arrangement for Ultra High-Density DRAMs", (Abstract), pps. 89-90.
		Hidaka et al., "A Divided/Shared Bit-Line Sensing Scheme for ULSI DRAM Cores", Journal of Solid-State Circuit, Vol. 26, No. 4, April 1991, pps. 473-477.

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Group Art Unit Unkn wn

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5,940,321	08/1999	Takeuchi et al.			
	5,949,698	09/1999	Shirley			
	6,005,265	12/1999	Kuroda et al.			
	6,018,172	01/2000	Hidaka et al.			
	6,034,879	03/2000	Min et al.			
	6,043,562	03/2000	Keeth			
	6,084,307	07/2000	Keeth			
	6,094,370	07/2000	Takashima			
	6,185,123	02/2001	Allen et al.			
	6,188,598	02/2001	Mueller et al.			
	6,222,275	04/2001	Keeth			
	6,243,311	06/2001	Keeth			

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OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

		IBM Technical Disclosure Bulletin, Vol. 30, No. 3, August 1987, pps. 1314-1315.
		IBM Technical Disclosure Bulletin, Vol. 30, No. 11, April 1988, pps. 246-248.

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	6,392,303	05/2002	Keeth			
	6,429,529	08/2002	Keeth			
	6,456,518	09/2002	Keeth			
	6,504,255	01/2003	Keeth			
	6,594,173	07/2003	Keeth			

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